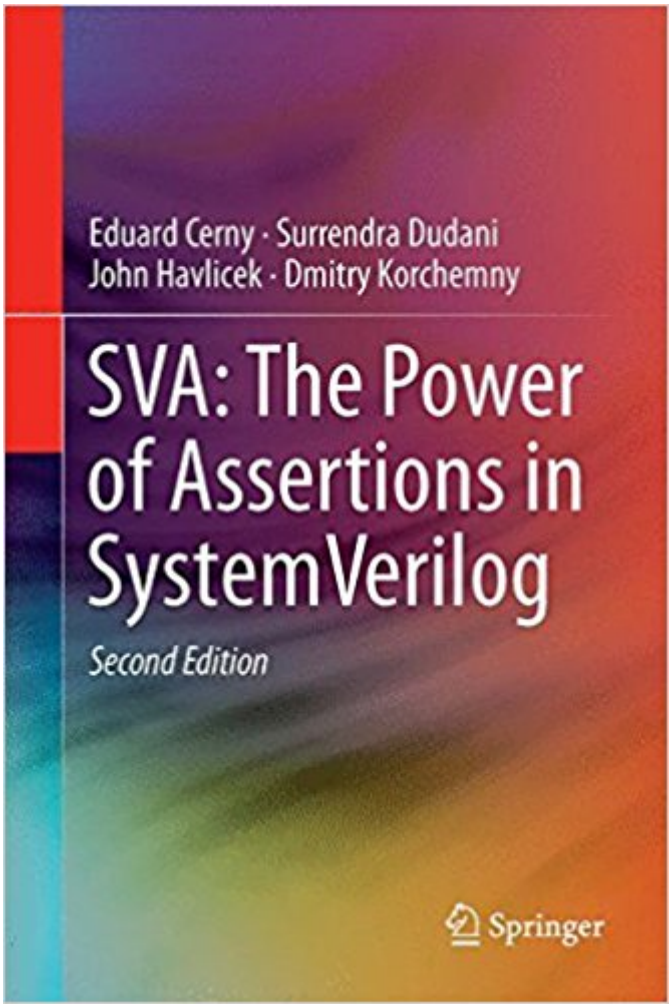
SVA: The Power Of Assertions In SystemVerilog



Synopsis

This book is a comprehensive guide to assertion-based verification of hardware designs using System Verilog Assertions (SVA). It enables readers to minimize the cost of verification by using assertion-based techniques in simulation testing, coverage collection and formal analysis. The book provides detailed descriptions of all the language features of SVA, accompanied by step-by-step examples of how to employ them to construct powerful and reusable sets of properties.Â The book also shows how SVA fits into the broader System Verilog language, demonstrating the ways that assertions can interact with other System Verilog components. The reader new to hardware verification will benefit from general material describing the nature of design models and behaviors, how they are exercised, and the different roles that assertions play. This second edition covers the features introduced by the recent IEEE 1800-2012.System Verilog standard, explaining in detail the new and enhanced assertion constructs. The book makes SVA usable and accessible for hardware designers, verification engineers, formal verification specialists and EDA tool developers. With numerous exercises, ranging in depth and difficulty, the book is also suitable as a text for students.

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step-by-step examples of how to employ them to construct powerful and reusable sets of properties. Â The book also shows how SVA fits into the broader SystemVerilog language, demonstrating the ways that assertions can interact with other SystemVerilog components. Â The reader new to hardware verification will benefit from general material describing the nature of design models and behaviors, how they are exercised, and the different roles that assertions play. Â This second edition covers the features introduced by the recent IEEE 1800-2012SystemVerilog standard, explaining in detail the new and enhanced assertion constructs. The book makes SVA usable and accessible for hardware designers, verification engineers, formal verification specialists, and EDA tool developers. Â With numerous exercises, ranging in depth and difficulty, the book is also suitable as a text for students.Â Â Â Â Â Â Â Â Â Â Â Provides a comprehensive guide to assertion-based verification with SystemVerilog Assertions (SVA);Â Â Â Â Â Â Â Â Â Â Includes step-by-step examples of how SVA can be used to construct powerful Â and reusable sets of properties;Â Â Â Â Â Â Â Â Â Â Covers the entire SVA language with all the recent enhancements of the IEEE 1800-2012 SystemVerilog standard.

Eduard Cerny received M.Eng. and Ph.D. degrees in electrical engineering from McGill University, Montreal, in 1970 and 1975, respectively. From 1978 until 2001 he was a professor in the Department Computer Science and Operations Research at the Universite de Montreal. He published and was a consultant in areas related to the specification, simulation, formal verification and test of microelectronics systems and in the development of CAD tools. He joined Synopsys, Inc., in 2001. Currently he is a Scientist in the Marlborough, MA, office as member of the Synopsys Verification Group. His responsibilities include design-for-verification methodology, in particular as related to assertions, with four patents in that area. He was co-chair and member of the IEEE P1800 System Verilog Assertions committee and a co-author of the books Verification Methodology Manual for System Verilog (Kluwer 2006) and The Power of System Verilog Assertions (Springer 2010).Surrendra Dudani received M.S. and Ph.D. degrees in electrical & computer engineering from Syracuse University, NY, in 1976 and 1980, respectively. From 1980 until 1989, he worked at Honeywell, Prime Computers and Stardent Computers as a Principal Engineer. He developed various design verification languages, CAD tools and methodologies. In 1990, he founded Pragmatics Computing to provide consulting services to hardware and software companies. He pioneered code coverage technology for design verification and introduced one of the first products in the market. He joined Synopsys, Inc., in 1999. Currently he is a Scientist in the Marlborough, MA, office as member of the Synopsys Verification Group. His current responsibilities include developing

and managing assertions technology and other techniques for design verification. He holds three patents and has published many papers at conferences. He was a member of the IEEE P1800 System Verilog Assertions committee and a co-author of The Power of System Verilog Assertions (Springer 2010).John Havlicek earned a B.S. in Mathematics from Ohio State (1987) and a Ph.D. in Mathematics from Stanford (1992). From 1996 to 2000, he pursued doctoral studies in Computer Sciences at the University of Texas, working on formal methods with E. Allen Emerson.Â He then joined Motorola Semiconductor and began work on tools and methodologies for semiconductor design verification.Â He has worked to expand the deployment of assertions both in simulation and formal verification and has been active in the creation and standardization of industrial assertion languages, notably IEEE 1850 PSL and IEEE 1800 System Verilog Assertions. He served as chair of the System Verilog Assertions Committee, served on the System Verilog Champions Committee and helped to found the System Verilog Discrete Committee. He was a primary author of enhancements to coverage modeling capabilities in the 2012 System Verilog standard. He also worked in a subgroup of the Verilog-AMS Committee to study assertion constructs for analog and mixed-signal verification. Currently, he works for Cadence Design Systems in the Design IP Team for DDR Memory Controller and PHY. As diversions, John enjoys early music, backpacking and amateur astronomy.Dmitry Korchemny earned an MSc. in electrical engineering and computer science from Moscow Institute of Radio-engineering, Electronics and Automation in 1984. He joined Intel in 1993. Currently he is a senior CAD technical staff engineer at Intel. His interests include pre- and post-Si verification, debug and test generation. He is actively involved into System Verilog Assertion standardization and he is a chair of Assertion Committee of IEEE P1800 Working Group.

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